ABSTRACT

A data interpolating device comprises plural stages of delay circuits (1_{-1}, 2_{-1}, 3_{-1}) for delaying discrete data sequentially inputted and multiplication/addition circuits (4_{-1} to 16_{-1}) that performs weighted addition of data outputted from the output stages of the plural stages of delay circuits (1_{-1}, 2_{-1}, 3_{-1}) according to the value of a digital basic function (-1, 1, 8, 8, 1, -1) and thereby determine interpolation data. Since a sampling function of finite supports differentiable once or more times over the whole range.